Silicon Carbide Substrates

Product Specifications

（Version:2024）

4H P-Type

6H P-Type

3C N-Type

Prepare/Date：10th -Jan-2023 **Check/Date**：9th-Sep-2024 **Approve/Date**：10th-Sep-2024

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SILICON CARBIDE MATERIAL PROPERTIES※

Propery	P-type 4H-SiC, Single Crystal	P-type 6H-SiC, Single Crystal	N-type 3C-SiC, Single Crystal
Lattice Parameters	a=3.082 Å c=10.092 Å	a=3.09 Å c=15.084 Å	a=4.349 Å
Stacking Sequence	ABCB	ACBABC	ABC
Mohs Hardness	≈9.2	≈9.2	≈9.2
Density	3.23 g/cm^3	3.0 g/cm^3	3.17 g/cm^3
Therm. Expansion Coefficient	4.3×10^{-6}/K(⊥*C* axis) 4.7×10^{-6}/K(∥*C* axis)	4.3×10^{-6}/K(⊥*C* axis) 4.7×10^{-6}/K(∥*C* axis)	3.8×10^{-6}/K
Refraction Index @750nm	n_o = 2.621 n_e = 2.671	n_o=2.612 n_e=2.651	n=2.615
Dielectrc Constant	c~9.66	c~9.66	c~9.66
Thermal Conductivity	3-5 W/cm·K@298K	3-5 W/cm·K@298K	3-5 W/cm·K@298K
Band-Gap	3.26 eV	3.02 eV	2.36 eV
Break-Down Electrical Field	2-5×10^{6}V/cm	2-5×10^{6}V/cm	2-5×10^{6}V/cm
Saturation Drift Velocity	2.0×10^{5}m/s	2.0×10^{5}m/s	2.7×10^{7}m/s

※ Silicon carbide material properties is only for reference.

APPLICATIONS

III-V Nitride Deposition

Optoelectronic Devices

High-Power Devices

High-Temperature Devices High-

Frequency Power Device

GENERAL DEFINITION

LABCDE-XXX

L– Standard

A – Diameter
- 2 – 50.8 mm (2 inch)
- 4 – 100.0 mm (4 inch)
- 6 – 150.0 mm (6 inch)
- 5 – 5.0*5.0 mm (Square)
- 7– 10.0*10.0 mm (Square)

B – property
- 1 – 3C type
- 2 – 4H type
- 3 – 6H type

C– Dopant
- N – Nitrogen
- P – Aluminum

D –Orientation
- 0 – On-axis
- 2 – 2° off axis
- 4 – 4° off axis

E – Grade
- Z – Zero MPD
- P – Product
- D – Dummy

X – Silicon face polish
- L – Lapping
- P – Optical polish
- C – CMP, EPI-ready

X – Carbon face polish
- L – Lapping
- P – Optical polish
- C – CMP, EPI-ready

X – Thickness
- E – 350 μm
- F – 500 μm
- X– Other thickness

Orientation of SiC substrate	
crystal orientation	Orientation crystallography of the SiC substrate the Angle of inclination between the c axis and the vector perpendicular to the wafer surface (see Figure 1).
Orthogonal orientation deviation	When the crystal face is intentionally deviated from the (0001) crystal face, the Angle between the normal vector of the crystal face projected on the (0001) plane and the direction [11-20] nearest to the (0001) plane.
off-axis	< 11-20 > Direction deviation 4.0°±0.5°
positive axis	<0001> Direction off 0°±0.5°

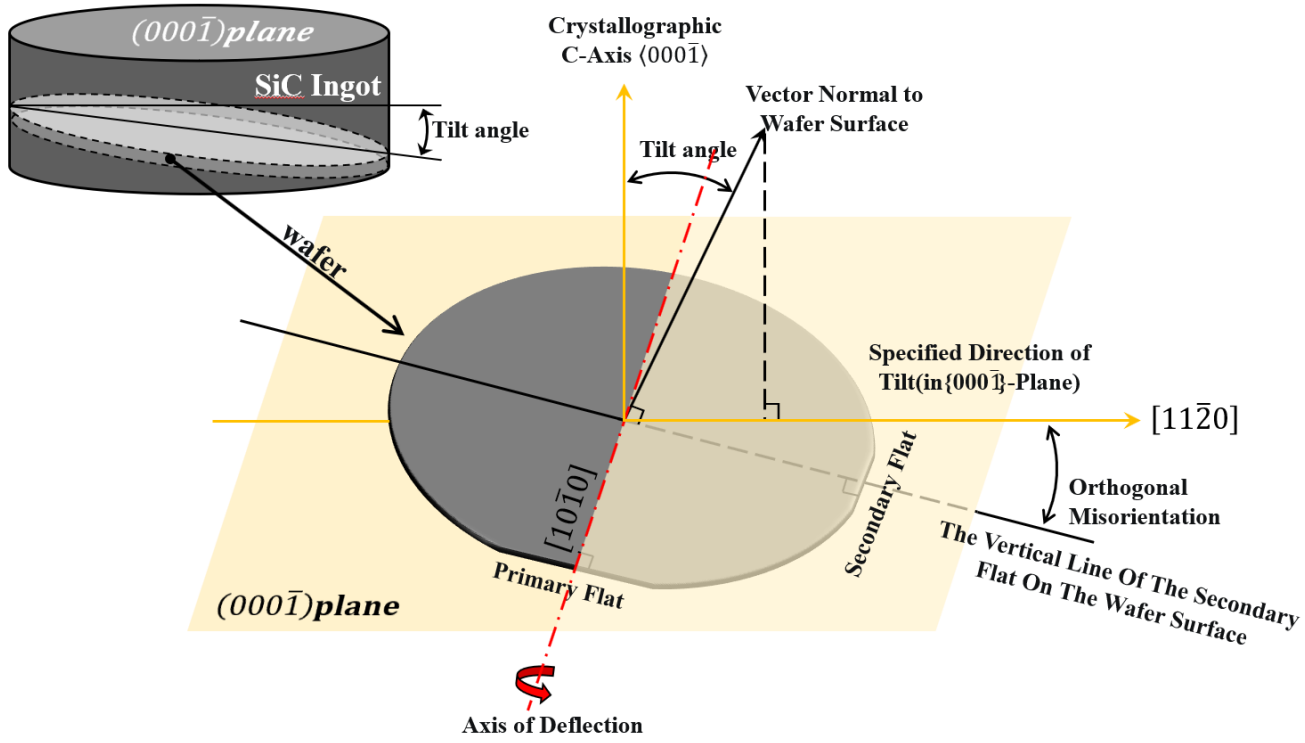

Figure.1 Orthogonal Misorientation

Diameter	Measure the wafer diameter with a standard vernier caliper (see Figure 2).
Primary Flat	The edge having the longest length on a wafer whose crystal surface is parallel to the {1010} lattice plane.
orientation of Primary Flat	The orientation of Primary Flat is always parallel to the < 1120 > direction (or parallel to the {1010} lattice plane). Primary Flat was measured by XRD back reflection technique
Secondary Flat	Its length is shorter than that of the main positioning edge, and its position relative to the Primary Flate can distinguish the Si and C surfaces (Figure 2).
orientation of Secondary Flat	With Si face up, the orientation of the Secondary Flat can be rotated 90° clockwise along the Primary Flat.
Marking	For Si surface polishing materials, the C surface of each wafer is marked with laser marking (Figure 2).

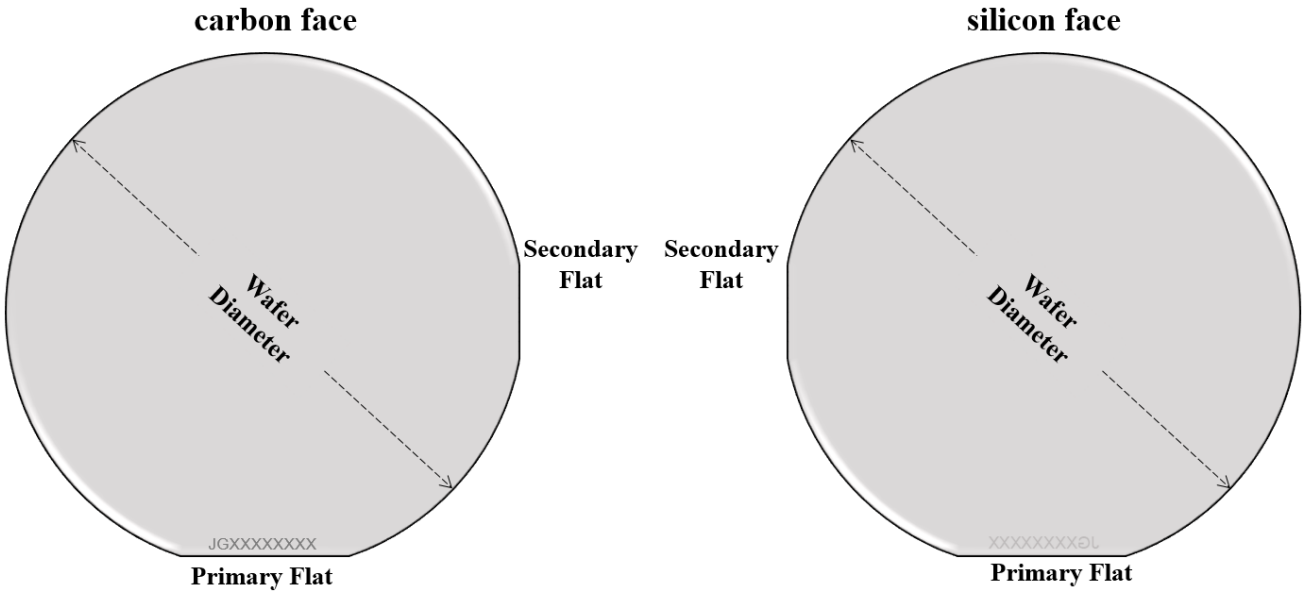

Figure 2 Schematic diagram of wafer C and Si face wafer diameter, Primary Flat, Secondary Flat and laser marking position.

晶格领域 6 英寸 SiC 晶片产品标准

6 inch diameter Silicon Carbide (SiC) Substrate Specification

等级Grade			精选级（Z 级）Zero MPD Production Grade (Z Grade)	工业级（P 级）Standard Production Grade (P Grade)	测试级（D 级）Dummy Grade (D Grade)
直径 Diameter			145.5 mm~150.0 mm		
厚度 Thickness			350 μm ± 25 μm		
晶片方向 Wafer Orientation			Off axis: 2.0°-4.0°toward [11$\bar{2}$0] ± 0.5° for 4H/6H-P, On axis: ⟨111⟩ ± 0.5° for 3C-N		
微管密度※ Micropipe Density			0 cm^{-2}		
电 阻 率※ Resistivity		p-type 4H/6H-P	≤0.1 Ω·cm		≤0.3 Ω·cm
		n-type 3C-N	≤0.8 mΩ·cm		≤1 m Ω·cm
主定位边方向 Primary Flat Orientation		4H/6H-P	{10$\bar{1}$0} ± 5.0°		
		3C-N	{1$\bar{1}$0} ± 5.0°		
主定位边长度 Primary Flat Length			47.5 mm ± 2.0 mm		
次定位边长度 Secondary Flat Length			None		
次定位边方向 Secondary Flat Orientation			Silicon face up: 90° CW. from Prime flat ± 5.0°		
边缘去除 Edge Exclusion			3 mm		6 mm
局部厚度变化/总厚度变化/弯曲度/翘曲度 LTV/TTV/Bow /Warp			≤2.5 μm/≤5 μm/≤15 μm/≤30 μm		≤10 μm/≤15 μm/≤25 μm/≤40 μm
表面粗糙度※ Roughness			Polish Ra≤1 nm		
			CMP Ra≤0.2 nm		Ra≤0.5 nm
边缘裂纹(强光灯观测) Edge Cracks By High Intensity Light			None		Cumulative length ≤ 10 mm, single length≤2 mm
六方空洞(强光灯测) ※ Hex Plates By High Intensity Light			Cumulative area ≤0.05%		Cumulative area ≤0.1%
多型(强光灯观测) ※ Polytype Areas By High Intensity Light			None		Cumulative area≤3%
目测包裹物(日光灯观测) Visual Carbon Inclusions			Cumulative area ≤0.05%		Cumulative area ≤3%
硅面划痕(强光灯观测) # Silicon Surface Scratches By High Intensity Light			None		Cumulative length≤1×wafer diameter
崩边(强光灯观测) Edge Chips High By Intensity Light			None permitted ≥0.2mm width and depth		5 allowed, ≤1 mm each
硅面污染物(强光灯观测) Silicon Surface Contamination By High Intensity			None		
包装 Packaging			Multi-wafer Cassette or Single Wafer Container		

Notes:

※ Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.

晶格领域 4英寸 SiC 晶片产品标准

4 inch diameter Silicon Carbide (SiC) Substrate

等级Grade			精选级（Z 级）Zero MPD Production Grade (Z Grade)	工业级（P 级）Standard Production Grade (P Grade)	测试级（D 级）Dummy Grade (D Grade)
直径 Diameter			99.5 mm~100.0 mm		
厚度 Thickness			350 μm ± 25 μm		
晶片方向 Wafer Orientation			Off axis: 2.0°-4.0°toward [11$\bar{2}$0] ± 0.5° for 4H/6H-P, On axis: 〈111〉 ± 0.5° for 3C-N		
微管密度※ Micropipe Density			0 cm^{-2}		
电 阻 率※ Resistivity		p-type 4H/6H-P	≤0.1 Ω·cm		≤0.3 Ω·cm
		n-type 3C-N	≤0.8 mΩ·cm		≤1 m Ω·cm
主定位边方向 Primary Flat Orientation		4H/6H-P	{10$\bar{1}$0} ± 5.0°		
		3C-N	{1$\bar{1}$0} ± 5.0°		
主定位边长度 Primary Flat Length			32.5 mm ± 2.0 mm		
次定位边长度 Secondary Flat Length			18.0 mm ± 2.0 mm		
次定位边方向 Secondary Flat Orientation			Silicon face up: 90° CW. from Prime flat ± 5.0°		
边缘去除 Edge Exclusion			3 mm		6 mm
局部厚度变化/总厚度变化/弯曲度/翘曲度 LTV/TTV/Bow /Warp			≤2.5 μm/≤5 μm/≤15 μm/≤30 μm		≤10 μm/≤15 μm/≤25 μm/≤40 μm
表面粗糙度※ Roughness			Polish Ra≤1 nm		
			CMP Ra≤0.2 nm		Ra≤0.5 nm
边缘裂纹(强光灯观测) Edge Cracks By High Intensity Light			None		Cumulative length ≤ 10 mm, single length≤2 mm
六方空洞(强光灯测) ※ Hex Plates By High Intensity Light			Cumulative area ≤0.05%		Cumulative area ≤0.1%
多型(强光灯观测) ※ Polytype Areas By High Intensity Light			None		Cumulative area≤3%
目测包裹物(日光灯观测) Visual Carbon Inclusions			Cumulative area ≤0.05%		Cumulative area ≤3%
硅面划痕(强光灯观测) # Silicon Surface Scratches By High Intensity Light			None		Cumulative length≤1×wafer diameter
崩边(强光灯观测) Edge Chips High By Intensity Light			None permitted ≥0.2mm width and depth		5 allowed, ≤1 mm each
硅面污染物(强光灯观测) Silicon Surface Contamination By High Intensity			None		
包装 Packaging			Multi-wafer Cassette or Single Wafer Container		

Notes:

※Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.

晶格领域 2 英寸 SiC 晶片产品标准

2 inch diameter Silicon Carbide (SiC) Substrate

等级 Grade			工业级 Production Grade (P Grade)	研究级 Research Grade (R Grade)	试片级 Dummy Grade (D Grade)
直径 Diameter			50.8mm±0.38mm		
厚度 Thickness			350 μm±25 μm		
晶片方向 Wafer Orientation			Off axis: 2.0°-4.0°toward [11$\bar{2}$0] ± 0.5° for 4H/6H-P, On axis: ⟨1$\bar{1}$1⟩ ± 0.5° for 3C-N		
微管密度 Micropipe Density			0 cm^{-2}		
电阻率 ※Resistivity	4H/6H-P		≤0.1 Ω·cm		
	3C-N		≤0.8 mΩ•cm		
主定位边方向 Primary Flat Orientation		4H/6H-P	{10-10} ±5.0°		
		3C-N	{1-10} ±5.0°		
主定位边长度 Primary Flat Length			15.9 mm ±1.7 mm		
次定位边长度 Secondary Flat Length			8.0 mm ±1.7 mm		
次定位边方向 Secondary Flat Orientation			Silicon face up: 90° CW. from Prime flat ±5.0°		
边缘去除 Edge Exclusion			3 mm		3 mm
总厚度变化/弯曲度/翘曲度 TTV/Bow /Warp			≤2.5 μm/≤5 μm/≤15 μm/≤30 μm		
表面粗糙度※ Roughness			Polish Ra≤1 nm		
			CMP Ra≤0.2 nm		
边缘裂纹(强光灯观测) Edge Cracks By High Intensity Light			None		1 allowed, ≤1 mm
六方空洞(强光灯观测) ※ Hex Plates By High Intensity Light			Cumulative area≤1 %		Cumulative area≤3 %
多型(强光灯观测) ※ Polytype Areas By High Intensity Light			None	Cumulative area≤2 %	Cumulative area≤5%
Si 面划痕(强光灯观测) # Silicon Surface Scratches By High Intensity Light			3 scratches to 1×wafer diameter cumulative length	5 scratches to 1×wafer diameter cumulative length	8 scratches to 1×wafer diameter cumulative length
崩边(强光灯观测) Edge Chips High By Intensity Light light			None	3 allowed, ≤0.5 mm each	5 allowed, ≤1 mm each
硅面污染物(强光灯观测) Silicon Surface Contamination By High Intensity			None		
包装 Packaging			Multi-wafer Cassette or Single Wafer Container		

Notes:

※Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.

晶格领域 5*5 & 10*10mm 英寸 SiC 晶片产品标准

5*5 & 10*10mm inch diameter Silicon Carbide (SiC)

等级 Grade			工业级 Production Grade (P Grade)	研究级 Research Grade (R Grade)	试片级 Dummy Grade (D Grade)
直径 Diameter			5*5mm±0.2mm & 10*10mm±0.2mm		
厚度 Thickness			350 μm±25 μm		
晶片方向 Wafer Orientation			Off axis: 2.0°-4.0°toward [11$\bar{2}$0] ± 0.5° for 4H/6H-P, On axis: ⟨1$\bar{1}$1⟩ ± 0.5° for 3C-N		
微管密度 Micropipe Density			0 cm^{-2}		
电阻率 ※Resistivity	4H/6H-P		≤0.1 Ω·cm		
	3C-N		≤0.8 mΩ•cm		
主定位边方向 Primary Flat Orientation		4H/6H-P	{10-10} ±5.0°		
		3C-N	{1-10} ±5.0°		
主定位边长度 Primary Flat Length			15.9 mm ±1.7 mm		
次定位边长度 Secondary Flat Length			8.0 mm ±1.7 mm		
次定位边方向 Secondary Flat Orientation			Silicon face up: 90° CW. from Prime flat ±5.0°		
边缘去除 Edge Exclusion			3 mm		3 mm
总厚度变化/弯曲度/翘曲度 TTV/Bow /Warp			≤2.5 μm/≤5 μm/≤15 μm/≤30 μm		
表面粗糙度※ Roughness			Polish Ra≤1 nm		
			CMP Ra≤0.2 nm		
边缘裂纹(强光灯观测) Edge Cracks By High Intensity Light			None		1 allowed, ≤1 mm
六方空洞(强光灯观测) ※ Hex Plates By High Intensity Light			Cumulative area≤1 %		Cumulative area≤3 %
多型(强光灯观测) ※ Polytype Areas By High Intensity Light			None	Cumulative area≤2 %	Cumulative area≤5%
Si 面划痕(强光灯观测) # Silicon Surface Scratches By High Intensity Light			3 scratches to 1×wafer diameter cumulative length	5 scratches to 1×wafer diameter cumulative length	8 scratches to 1×wafer diameter cumulative length
崩边(强光灯观测) Edge Chips High By Intensity Light light			None	3 allowed, ≤0.5 mm each	5 allowed, ≤1 mm each
硅面污染物(强光灯观测) Silicon Surface Contamination By High Intensity			None		
包装 Packaging			Multi-wafer Cassette or Single Wafer Container		

Notes:

※Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.